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Response to Office action 3/10/2006
Response submitted March 28, 2006

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1 - 9 remain in the application. Claims 1, 3, 5, 6 and 7 have been amended.

Claim 6 has been amended in light of the rejection under 35 U.S.C. § 112. The modifier "substantially" has been deleted, so that the backup is implemented "automatically."

The specification and the claims meet the requirements of 35 U.S.C. § 112, first and second paragraphs. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved.

We now turn to the art rejection, in which claims 1, 2, 7, and 8 have been rejected as being anticipated by Johnson et al. (US 2003/0033477, "Johnson") under 35 U.S.C. § 102 and claims 3-6 have been rejected as being obvious over the combined teachings of Johnson et al. and Brahmarouthu (*Intel Developer Update Magazine, Aug. 2002*) under 35 U.S.C. § 103. We respectfully traverse.

The independent claims have all been amended in response to the rejection. The serial ATA cable connection between the processor and the intermediate adapter has been incorporated into these claims. Support is found, for example, in the original claim 3, in the specification on page 9, para. [0032], and in the drawing figure. The serial ATA connection is identified with reference numeral "2."

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Johnson shows a processor ("system 204") that outputs to a RAID controller 202.

The data engine 216 in the RAID controller distributes the data to several drives 206

. . . 212. As explained by Johnson:

> The present invention may be practiced with a variety of Message
> Passing Technology (MPT) controllers, including Serial Attached Small
> Computer Systems Interface (SAS), Serial Advanced Technology
> Attachment (SATA), Parallel Advanced Technology Attachment
> (PATA), Fiber . . . .

Johnson, p. 2, para. [0022] (emphasis added). That is, serial ATA is one of the

possible connections between the RAID controller and the storage drives.

Johnson is silent with regard to the connection between the processor and the RAID

controller. Johnson did not even identify or make any special mention of the double-

arrow connection between his boxes 204 and 202. Most likely, one would assume,

the connection is effected through the PCI bus. There is no teaching – or even a hint

– that Johnson was concerned at all with the connection between the processor and

the RAID controller. Accordingly, Johnson does not anticipate the claimed invention.

The foregoing was also recognized by the Examiner. The reference Brahmarouthu

was accordingly added in the rejection of claims 3-6. The secondary reference

describes the virtues of connecting to the motherboard via serial ATA. Page 4, for

example, shows a picture of parallel connectivity juxtaposed to a picture of serial

connectivity. There are two primary differences between the parallel and serial

connections: First, the data transfer speed is increased. Parallel ATA is limited to

100 MB/s while serial ATA transfers at 150 MB/s even in the first generation (with

future increases to 300 and even 600 MB/s). Second, serial connectivity uses much

smaller connectors and, accordingly, "board real estate" required for the SATA

connectors is reduced to 25% as opposed to PATA. See, Brahmarouthu, page 4.

Brahmarouthu connects his disk drives to the board via the serial ATA connectors. In

fact, most *Intel* boards now come with several serial ATA connectors (see, *Intel*

Desktop Board D915PGN) for connecting the disk drives. This does not suggest —

nor does the secondary reference hint at — connecting an intermediate adapter that

distributes the data from the processor to a plurality of drives.

It is also telling that a serial ATA cable connection allows only a <u>single</u> drive to be

connected. The seven leads (3 GND and 2 pairs of differential signals) can only

address a single drive, as opposed, for example, to parallel ATA that allows two

drives or SCSI that allows several slave drives. Fact is that the serial ATA spec calls

for point-to-point connection. Such point-to-point connectivity, therefore, teaches

away from applicant's solution.

At this point, we must consider the "motivation" that would prompt a person of skill in

the art to combine Johnson and Brahmarouthu. Johnson's connection between the

processor and the RAID controller is (most likely) through the PCI bus. Accordingly,

neither the speed issue nor the "real estate" issue come into play. Even the first

generation of the PCI bus transferred at over 130 MB/s (e.g. 32 bit bus at 33 MHz)

and current PCI versions transfer at multiples thereof. The PCI bus connector and

expansion slots are still available, even where the serial ATA connectors are

provided (see, e.g., *Intel Desktop Board D915PGN*).

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If a RAID system were integrated, say, in the right-hand picture of Brahmarouthu,

one would <u>obviously</u> plug the RAID controller into the PCI connector slot, and then

connect the multiple drives to the RAID controller via serial ATA cables. Again, this is

no different from Johnson, where the RAID controller connects to the drives via serial

ATA (as one of several options). It would, therefore, be much more obvious to

continue using the PCI connection to add in a RAID controller. The art does not

teach away from such a configuration. Specifically, Brahmarouthu does <u>not</u> teach a

serial ATA connection between a motherboard (processor) and an intermediate

adapter (e.g., RAID controller).

In summary, none of the references, whether taken alone or in any combination,

either show or suggest the features of claims 1, 5, or 7. These claims are, therefore,

patentable over the art and since all of the dependent claims are ultimately

dependent thereon, they are patentable as well. In view of the foregoing,

reconsideration and the allowance of claims 1 - 9 are solicited.

Respectfully submitted,

For Applicant

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